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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,074	10/23/2003	Nhon Quach	42390.P7442C	2223

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EXAMINER	
ROJAS, MIDYS	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,074	QUACH ET AL.	
	Examiner	Art Unit	
	Midys Rojas	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/23/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 10/23/03 has been considered by the examiner.

The reference cited on this IDS, titled "Motorola MC88110 Second Generation RISC Microprocessor User's Manual" has not been considered since this reference was not provided to the examiner by the applicant.

Drawings

2. The drawings filed on 10/23/03 have been accepted by the examiner.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re*

Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-5 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-3, 8 of U.S. Patent No. 6,711,653. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims of the instant application are broader than those of Patent No. 6,711,653; thus, the Patent in question reads on the claims of the instant application as illustrated below.

Instant Application – 10/693,074	Patent 6,711,653
Claim 1- A processor comprising: a translation-lookaside-buffer (TLB); a cache to provide temporary storage for a data	Claim 1 – A processor comprising: a translation-lookaside-buffer (TLB); a cache to provide temporary storage for a data

block; and a memory management unit to implement a first cache-coherency mechanism if the processor is in a first mode and to implement a second cache-coherency mechanism if the processor is in a second mode.	block; a memory management unit to implement a first cache-coherency mechanism if the processor is in a first mode and to implement a second cache-coherency mechanism if the processor is in a second mode, wherein the second cache coherency ...
Claim 2 – The processor of claim 1, wherein the TLB includes a plurality of entries, each entry including a virtual address tag, a physical address, and a memory attribute.	Claim 2 – The processor of claim 1, wherein the TLB includes a plurality of entries, each entry including a virtual address tag, a physical address, and a memory attribute.
Claim 3 – The processor of claim 2, wherein the first cache coherency mechanism snoops the cache if an access to a memory address designated by an uncacheable memory attribute is detected.	Claim 3 – The processor of claim 2, wherein the first cache coherency mechanism snoops the cache if an access to a memory address designated by an uncacheable memory attribute is detected.
Claim 4 – A computer system comprising: an execution core; a cache having a plurality of data entries; a memory to store an operating system for the	Claim 8 – A computer system comprising: an execution core; a cache having a plurality of data entries; a memory to store an operating system for the

computer system; and a memory management unit to manage data flow among the execution core, the cache and the memory, the memory controller to operate in a first cache coherency mode or a second cache coherency mode according to a property of the operating system.	computer system; a memory management unit to manage data flow among the execution core, the cache and the memory, the memory controller to operate in a first cache coherency mode or a second cache coherency mode according to a property of the operating system, wherein the first cache coherency mode supports memory attribute aliasing and the second cache coherency mode does not support memory attribute aliasing, wherein…
Claim 5 – The computer system of claim 4, wherein the first cache coherency mode supports memory attribute aliasing and the second cache coherency mode does not support memory attribute aliasing.	Claim 8 – … wherein the first cache coherency mode supports memory attribute aliasing and the second cache coherency mode does not support memory attribute aliasing…

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 4 is rejected under 35 U.S.C. 102(b) as being anticipated by Krick (5,781,774).

Krick discloses a computer system (Figure 3) comprising: an execution core (Processor Core 60); a cache having a plurality of data entries (Cache memory 70); a memory to store an operating system for the computer system (within processor 60); and a memory management unit to manage data flow among the execution core, the cache and the memory (12), the memory controller to operate in a first cache coherency mode or a second cache coherency mode according to a property of the operating system (...processor that enables and disables... cache coherency mechanisms according to an operating mode determined by an input pin, Col. 2, lines 23-26).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krick (5,781,774) in view of Applicant's Admitted Prior Art.

Regarding Claim 1, Krick discloses a processor (Figure 3, Processor Core 60) comprising: a cache having a plurality of data entries (Cache memory 70); a memory to store an operating system for the computer system (within processor 60); and a memory management unit (12) to implement a first cache-coherency mechanism if the processor is in a first mode and to implement a second cache-coherency mechanism if the processor is in a second mode

(...processor that enables and disables... cache coherency mechanisms according to an operating mode determined by an input pin, Col. 2, lines 23-26). Krick does not teach the system having a TLB. Applicant's Admitted Prior Art discloses the use if a TLB for storing physical address translations of recently reference logical addresses (Page 3, paragraph 005). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Krick with the TLB of Applicant's Admitted Prior Art since having this TLB would allow for faster access to recently referenced address translations since the TLB is closer to the processor core.

Regarding Claim 2, Applicant's Admitted Prior Art discloses a TLB including a plurality of entries, each entry including a virtual address tag, a physical address (each needed in order to hold physical address translations), and a memory attribute (page 3, paragraph 005).

Regarding Claim 3, Krick discloses the processor wherein the first cache coherency mechanism snoops the cache if an access to a memory address designated by an uncacheable memory attribute is detected (Col. 5, lines 24-28).

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Krick (5,781,774) in view of Wing et al. (5,926,832).

Krick discloses the invention as described in Claim 1 above. Krick does not teach the first cache coherency mode supports memory attribute aliasing and the second cache coherency mode does not support memory attribute aliasing. Wing discloses the setting of a mode in register 128, which indicates when aliasing is enabled or disabled (Col. 27, lines 20-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the aliasing detection of Wing et al. in the system of Krick since doing so allows

optimizations that eliminate loads and stores. This ultimately enables better scheduling of operations in a machine with parallel execution resources (Wing, Col. 27, lines 59-65).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Rojas whose telephone number is (571) 272-4207. The examiner can normally be reached on M-F 5:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Midys Rojas
Examiner
Art Unit 2185

MR

Mano Padmanabhan
3/20/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER